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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,144	01/31/2002	Takao Yonehara	00862.022498	5995

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,144	YONEHARA ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of the Group I invention, claim(s) 1-10 in the response filed on November 3, 2003, is acknowledged. The traversal is on the ground(s) that "there would not be undue burden in examining the two groups of claims in a single application. In particular, MPEP § 808 makes clear that in order to require restriction between independent or distinct inventions, reasons for insisting upon a restriction requirement, such as undue burden, must also be shown. In the present instance, it is not believed that there would be undue burden in examining the two groups of claims in a single application, since the two groups of claims are not so different as would require a burden on the Examiner that is significantly beyond that of the normal burdens of examination." This is not found persuasive. A restriction requirement between one set of product claims and a set of process claims was issued in the Office action that was mailed on September 29, 2003. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds that "the product as claimed can be made by another and materially different process such as a process wherein ion implantation process can be performed instead of using pressure of a fluid during separation step of separating the member at separation layer in order to process device of Group II, (i.e., Smart Cut process)" and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being distinct, the examiner indicated that restriction is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore **made FINAL**.

2. Claims 11 and 12 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed in the response filed on November 3, 2003.

Priority

3. Acknowledgment is made of applicants' claim for foreign priority based on an application filed in Japan on January 31, 2001. It is noted, however, that applicant has not filed a certified copy of the 2001-023847 application as required by 35 U.S.C. 119(b).

Status of the Claims

4. Claims 1-12 are pending in the application.

5. Claims 11 and 12are withdrawn form further consideration by the examiner as indicated in Paragraph 2 herein above.

6. Claims 1-10 are treated on the merits as set forth herein below.

Drawings

7. Figures 6A-6C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --METHOD OF MANUFACTURING THIN-FILM SEMICONDUCTOR DEVICE--.

Claim Objections

9. Claims 1 and 10 are objected to because of the following informalities:

Claim 1 recites the limitation "the step of preparing a member" in line 3. The Examiner suggests to change "**the** step of preparing a member" to -- **a** step of preparing a member-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim 1 recites the limitation "the separation step of separating" in line 6. The Examiner suggests to change "**the** separation step of separating" to -- **a** separation step of separating-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim 1 recites the limitation "the chip forming step" in line 8. The Examiner suggests to change "**the** chip forming step" to -- **a** chip forming step-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim 10 recites the limitation "the step of preparing a member" in line 3. The Examiner suggests to change "**the** step of preparing a member" to -- **a** step of preparing a member-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim 10 recites the limitation "the chip forming step" in line 6. The Examiner suggests to change "**the** chip forming step" to -- **a** chip forming step-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim 10 recites the limitation "the separation step" in line 8. The Examiner suggests to change "**the** separation step" to -- **a** separation step-- in order to establish proper antecedent basis. Appropriate correction is required.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1-7 and 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 6,677,183. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

Re claim 1, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. The limitations include a method of manufacturing a thin-film semiconductor device, comprising: the step of preparing a member having a semiconductor film with a semiconductor element semiconductor integrated circuit on a separation layer (see Claim 1, lines 1-5); the separation step of separating the member at the separation layer by a pressure of a fluid (see Claim 1, lines 8-13); and the chip forming step after the separation step, forming the semiconductor film into chips (see Claim 15, lines 1-2).

Re claim 2, as applied to claim 1 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. In addition, the limitations wherein the member is obtained by forming a porous layer on a surface of a semiconductor substrate, forming the semiconductor film on a surface of

the porous layer, and then forming the semiconductor element and/or semiconductor integrated circuit is clamed in Claim 3 of U.S. Patent No. 6,677,183 (see Claim 3, lines 1-5).

Re claim 3, as applied to claims 1 and 2 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 3, and 15 of U.S. Patent No. 6,677,183. Further the limitation, wherein the semiconductor film is formed on the surface of the porous layer after forming a protective film on inner walls of pores in the porous layer is claimed in Claim 4 of U.S. Patent No. 6,677,183 (see Claim 4, lines 1-6).

Re claim 4, as applied to claim 1 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. Furthermore, the limitation, wherein the member is obtained by forming the semiconductor element and/or semiconductor integrated circuit on a surface of a semiconductor substrate and implanting ions from the surface side to a predetermined depth to form the separation layer is claimed in Claim 18 of U.S. Patent No. 6,677,183 (see Claim 18, lines 12-16).

Re claim 5, as applied to claims 1 and 2 above the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 3, and 15 of U.S. Patent No. 6,677,183. Further the limitation, wherein the semiconductor substrate is a single-crystal silicon substrate or a compound semiconductor substrate is claimed in Claim 5 of U.S. Patent No. 6,677,183 (see Claim 5, lines 1-3).

Re claim 6, as applied to claims 1 and 4 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 15 and 18 of U.S. Patent No. 6,677,183. In addition, the limitation wherein the semiconductor substrate is a

single-crystal silicon substrate or a compound semiconductor substrate is claimed in Claim 5 of U.S. Patent No. 6,677,183 (see Claim 5, lines 1-3).

Re claim 7, as applied to claims 1, 2 and 5 above, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1, 3, and 15 of U.S. Patent No. 6,677,183. Further, the limitation wherein the separation step is executed by applying the pressure of the fluid to the separation layer also claimed in Claims 10, 12 and 13 of U.S. Patent No. 6,677,183 (see Claim 10, lines 1-6, Claim 12, lines 1-3, Claim 13, lines 1-3).

Re claim 10, the scope of the claimed limitation of the instant application is essentially the same as the claimed limitations of claims 1 and 15 of U.S. Patent No. 6,677,183. The limitations include a method of manufacturing a thin-film semiconductor device, comprising: the step of preparing a member having a semiconductor film with a semiconductor element and/or semiconductor integrated circuit on a separation layer (see Claim 1, lines 8-13); the chip forming step of forming the member into chips in desired regions; and the separation step of, after the chip forming step, separating the member at the separation layer (see Claim 15, lines 1-2).

Therefore, the conflicting claims are not patentably distinct from each other.

Allowable Subject Matter

12. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art

of record does not teach "wherein after the separation step, the separation layer remaining on the semiconductor film side is removed, and then, the chip forming step is executed," as recited in claim 8 and "wherein after the separation step and the chip forming step, the step of removing the separation layer remaining on the semiconductor film side is executed," as recited in claim 9.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Fonstad, Jr. et al. (US/6,455,398), Nakagawa et al. (US/6,500,731), Fukunaga (US/6,602,761), and Iwane et al. (US/6,682,9900) also disclose similar inventive subject matter.

Fonstad, Jr. et al. (US/6,455,398) discloses method of bonding a silicon substrate to group III-V material substrate, the method includes annealing the substrate and thinning the substrate.

Nakagawa et al. (US/6,500,731) disclose a method of fabricating a semiconductor device a method includes forming a porous separation layer having prularity semiconductor layers which the semiconductor device separately formed on each the semiconductor layers.

Fukunaga (US/6,602,761) discloses process for fabricating an SOI substrate and the process includes forming single crystal silicon substrate and anodizing the single silicon substrate in order to form porous regions.

Iwane et al. (US/6,682,9900) disclose separation method of semiconductor layer and producing a solar cell.

However, the prior art fail to anticipate or render obvious the claimed limitation of the instant application as recited in claims 8 and 9 either taken alone or in combination.

Correspondence

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
February 2, 2004